IN THE SPECIFICATION

Amend paragraphs 11, 12, 14, 29, 44, 57, 60, 72, 81, 102, 106, 107, 110, 112, 113, and 117 as follows:

[0011] The timing of the voltages applied to the FET is controlled according to the invention so that, in an instance where the FET is to remain in the erased condition, the select voltage starts changing from its nominal value to the programming-enable value after the second voltage starts changing from its nominal value to the programming-inhibit value. The select voltage also preferably starts changing from its nominal value to the programming-enable value after the first voltage starts changing from its nominal value to its programming value and, if the control gate is present, after the control voltage starts changing from its nominal value to its programming value. Controlling ~~As a result, the FET goes into the programmed condition if the second voltage stays at its nominal value. If the second voltage goes to its programming inhibit value, controlling~~ the voltages applied to the FET in this way strongly ensures that the FET remains in the erased condition without moving significantly toward the programmed condition.

[0012] To see why the programming technique of the invention is advantageous, consider what would happen if the FET were intended to remain in the erased condition in the situation where the select voltage starts ~~start to~~ changing from its nominal value to the programming-enable value at approximately the same time that the first, second, and control voltages start changing from their nominal values to their various programming and programming-inhibit values. Under these circumstances, the first, select, and control voltages might sometimes change sufficiently faster than the second voltage that the FET temporarily turns on. Charge carriers would temporarily flow from the second source/drain region to the first source/drain region.

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[0014] In the preceding comparative circumstances where the select voltage starts changing at approximately the same time that the first, second, and control voltages start changing, the select and second voltages might sometimes change sufficiently faster than the first voltage that the FET turns on in the opposite direction from that indicated earlier. The resultant charge-carrier flow from the first source/drain region to the second source/drain region would again unnecessarily consume power. The present invention avoids these

program-disturbance and power-consumption difficulties by suitably delaying the point at which the select voltage changes from its nominal value to the programming-enable ~~its programming inhibit~~ value so that the FET does not temporarily turn on when it is intended to remain in the erased condition.

[0029] Fig. 1 illustrates part of a flash EPROM configured in accordance with the invention to avoid programming disturbances and unnecessary power consumption during programming operations. Fig. 2 depicts a partial implementation of the EPROM of Fig. 1 and further shows the basic architecture of the control circuitry that achieves the above-mentioned ~~preceding~~ advantages of the invention.

[0044] After erasure is completed, data can be written into the EPROM sector of Figs. 1 and 2. Writing is accomplished by performing a programming (or programming/write) operation on certain selected ones of floating-gate FETs 20 to place those selected FETs 20 in the programmed condition at logic "0" with their programmable threshold voltages (a) greater than second transition value V_{T2} if FETs 20 are of n-channel type or (b) less than $-V_{T2}$ if FETs 20 are of p-channel type. A programming operation consists of a main programming portion and a discharge portion. At the end of a typical programming ~~programming/write~~ operation, some of FETs 20 are typically in the programmed condition at logic "0" while others remain in the erased condition at logic "1". A read operation can then be performed to determine the data stored in various ones of FETs 20.

[0057] Control-line decoder 46 is connected to low-voltage generator 48 via a line 66 for receiving an erasure control voltage signal V_{CE} that reaches a low erasure control value V_{CEL} considerably below V_{SS}. Erasure control value V_{CEL} is typically 10 V below V_{SS}. Generator 48, normally implemented with a charge pump, generates erasure control voltage V_{CE} in response to a generator control signal V_{CLC}. In producing erasure control voltage V_{CE}, generator 48 may interact with bit-line decoder 58 and high-voltage generator 60 as described in Park, co-filed U.S. patent application 10/780,030, ~~__________, attorney docket no. R-0004 US,~~ the contents of which are incorporated by reference herein.

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[0060] Responsive to row address signals V_{RAD}, control-line selection signals V_{CLS}, erasure control voltage V_{CE}, and programming control voltage V_{CP}, control-line decoder 46 provides control-line (or control-gate or simply control) programming/erasure voltage signals

V_{CL} respectively on local control lines 70. Some of lines 70 are local to the EPROM sector illustrated in Figs. 1 and 2 while other lines 70 are local to other EPROM sectors. Each control line 70 for the illustrated EPROM sector is connected to control gates CG in one or more, typically four, rows of FETs 20 for providing an associated one of control-line programming/erasure voltages V_{CL} to those gates CG. Each cell row connected to a particular control line 70 is connected to a different source line 64. ~~62.~~ Decoder 46 in cooperation with generators 48 and 50 constitutes control-line (or control-gate) control circuitry that controls control-line voltages V_{SG}.

[0072] Body-line decoder 58 is connected to high-voltage generator 60 via a line 82 for receiving an erasure body voltage signal V_{BE} that reaches a high erasure body value V_{BEH} considerably greater than V_{DD}. Erasure body value V_{BEH} is typically 5 V above V_{DD} and thus typically 8 V above V_{SS}. Generator 60, normally implemented with a charge pump, generates erasure body value V_{BE} in response to a generator control signal V_{BHC}. In producing erasure body voltage V_{BE}, generator 58 may interact with control-line decoder 46 and low-voltage generator 48 as described in Park, U.S. patent application 10/780,030 ~~__________, attorney docket no. R-0004 US,~~ cited above.

[0081] Control-line decoder 46 consists of a control-line driver 102 and a core control-line decoder 104. In response to programming control voltage V_{CP}, erasure control voltage V_{CE}, and certain of control-line selection signals V_{CLS}, control-line driver 102 drives a line 106 ~~100~~ that carries a control-line driver voltage signal V_{CLD} provided to core control-line decoder 104. Driver 102 causes control-line driver voltage V_{CLD} to go from V_{SS} to V_{CPH} at a selected time during the main portion of a programming operation and to return to V_{SS} at a later selected time during the discharge portion. Responsive to driver voltage V_{CLD} and certain of selection signals V_{CLS}, core decoder 104 decodes row address signals V_{RAD} to produce control-line voltages V_{CL}.

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[0102] The length $t_C - t_1$ of the main portion of a programming operation is 10 - 15 μs, typically 12 μs, for the situation in which percentage-target-attainment voltages V_{ST} and V_{CT} are utilized to enable selected select-gate voltage V_{SG} to start rising at time t_A during the rises of selected voltages V_{SL} and V_{CL}. For this situation, the total rise time (t_1 to the latest of t_2 - t_4) of selected voltages V_{SL}, V_{CL}, and V_{SG} and each unselected bit-line voltage V_{DL} is 1 - 5 μs, typically 2 μs. Hence, selected voltages V_{SL}, V_{CL}, and V_{SG} and each unselected voltage

V_{DL} are jointly at their respective high values V_{SPH}, V_{CPH}, V_{ITM}, and V_{DD} for 8 - 12 μs, typically 10 μs. The total fall time (t_C to the latest of t_D and t_6 - t_8) of selected voltages V_{SL}, V_{CL}, V_{SG} and each unselected voltage V_{DL} is 0.5 - 2 μs, typically 1 μs. This is also the effective length of the discharge portion.

[0106] In the comparative example of Fig. 7, selected voltage V_{SG} applied to select gate SG of an unselected FET 20 exceeds unselected <u>bit-line</u> voltage V_{DL} applied to drain D by at least the 1-V fixed threshold voltage of the regular-FET portion of that FET 20 during the time period indicated by item 120 because selected <u>select-gate</u> voltage V_{SG} starts rising at the same time as unselected voltage V_{DL}. Inversion layer ID forms in unselected FET 20 during that time period. Selected voltage V_{CL} applied to control gate CG of unselected FET 20 exceeds unselected <u>bit-line</u> voltage V_{DL} by at least the erased value of the programmable threshold voltage of that FET 20 during at least part of the time period represented by item 120 in the comparative example of Fig. 7. Accordingly, inversion layer IS also forms in unselected FET 120 during at least part of that time period. Since inversion layer ID is also formed, unselected FET 20 is turned on during at least part of the time period represented by item 120.

[0107] Selected voltage V_{SL} applied to source S of unselected FET 20 in the comparative example of Fig. 7 exceeds unselected <u>bit-line</u> voltage V_{DL} during the time period represented by item 120 so that electrons flow from drain D of that FET 20 to source S during at least part of that time period. With selected <u>control-line</u> voltage V_{CL} being relatively high compared to unselected <u>bit-line</u> voltage V_{DL} during the time period represented by item 120, some of the electrons are drawn into floating gate FG. This increases the programmable threshold voltage of unselected FET 20 and moves its programmable threshold voltage away from the initial erased value and toward the programmed value to create a programming disturbance.

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[0110] Unselected <u>bit-line</u> voltage V_{DL} applied to drain D of unselected FET 20 exceeds selected source-line voltage V_{SL} in the comparative example of Fig. 9. Since unselected FET 20 is turned on during at least part of the time period represented by item 122, electrons flow from source S of that FET 20 to its drain D during at least part of that time period. Although no programming disturbance occurs in the comparative example of Fig. 9, the source-to-drain electron flow during the programming operation unnecessarily consumes power.

[0112] Figs. 10 and 11 deal with the discharge portion of a programming operation in which unselected bit-line voltage V_{DL} ~~VDL~~ drops considerably faster than each of selected voltages V_{SG}, V_{SL}, and V_{CL}. ~~VSG, VSL, and VCL.~~ Similar to what occurs in the comparative example of Fig. 7, these programming conditions cause unselected FET 20 to be turned on during at least part of the time period represented by item 124 in the comparative example of Fig. 11 because selected select-gate voltage V_{SG} ~~VSG~~ starts falling at the same time as unselected bit-line voltage V_{DL} ~~VDL~~ and selected voltages V_{SL} and V_{CL}. ~~VSL and VSG.~~ Electrons flow from drain D of unselected FET 20 to its source S in the comparative example of Fig. 11. As a result, unselected FET 20 in the comparative example of Fig. 11 undergoes a programming disturbance and unnecessarily consumes power. By arranging for selected select-gate voltage V_{SG} ~~VSG~~ to start falling sufficiently before unselected bit-line voltage V_{DL} ~~VDL~~ and selected voltages V_{SL} and V_{CL} ~~VSL and VCL~~ start falling as presented in the inventive example of Fig. 10., the EPROM of Figs. 1 and 2 substantially avoids programming disturbances and unnecessary power consumption that arise in the comparative example of Fig. 11.

[0113] Figs. 12 and 13 deal with the discharge portion of a programming operation in which selected source-line voltage V_{SL} drops faster than unselected bit-line voltage V_{DL}, selected select-gate voltage V_{SG}, and selected control-gate voltage V_{CL}. Analogous to what occurs in the comparative example of Fig. 9, these discharge conditions cause unselected FET 20 to be turned on during at least part of the time period represented by item 126 in the comparative example of Fig. 13 because, as in the comparative example of Fig. 11, selected select-gate voltage V_{SG} starts falling at the same time as selected voltage V_{SL}, unselected voltage V_{DL}, and selected voltage V_{CL}. Although no programming disturbance occurs in the comparative example of Fig. 13, electrons flow from source S of unselected FET 20 to its drain D. The resulting unnecessary power consumption is substantially avoided in the inventive example of Fig. 12 by having selected select-gate voltage V_{SG} start falling sufficiently before selected voltage V_{SL}, unselected voltage V_{DL}, and selected voltage V_{CL} start falling.

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[0117] The present invention has been described with reference to particular embodiments solely for the purpose of illustration. For instance, the present programming technique can be used in devices other than EPROMs. The definitions of the programmed

condition as the low logic state, e.g., logic "0", and the erased condition as the high logic state, e.g. logic "1", are arbitrary and can be reversed. Since source/drain regions S and D of each floating-gate memory FET 20 are specifically referred to respectively as source S and drain D only for convenience, source-line voltage V_{SL} and bit-line voltage V_{DL} at source S and drain D of each FET 20 can be respectively more generally referred to as first and second voltages respectively at first source/drain region S and second source/drain region D of that FET 20.

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